In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Previously presented)A signal processing apparatus, comprising:

a time-interleaved system operable to distribute a signal into a first processing pathway and, following a predetermined amount of time, into a second processing pathway; and

a delay structure coupled to said second processing pathway, said delay structure including at least one floating-gate field effect transistor,

wherein the predetermined amount of time depends on an amount of electrical charge stored on the floating gate of the at least one floating-gate field effect transistor, said amount of electrical charge adjusting a slew rate of an output of the delay structure to thereby controllably influence a triggering time of a circuit associated with at least one of the first and second processing pathways.

2. (Original) The signal processing apparatus of claim 1 wherein the signal processing apparatus comprises an analog-to-digital converter.

3. (Original) The signal processing apparatus of claim 1 wherein the signal processing apparatus comprises a quadrature mixing circuit.

4. (Previously presented)A signal processing apparatus, comprising:

an input node configured to receive a signal;

a splitter operable to split the signal into a first signal portion and a second signal portion and direct the first signal portion to a first node and directing the second signal portion to a second node; and

a first circuit coupled between said first node and a third node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an amount of electrical charge stored on a floating gate of said first transistor, said amount of electrical charge adjusting a slew rate of an output of the first circuit to thereby controllably influence a triggering time of a circuit associated with the third node.

5. (Original) The signal processing apparatus of claim 4, further comprising a second circuit coupled between said second node and a fourth node.

6. (Original) The signal processing apparatus of claim 5, further comprising a combiner operable to combine signals from outputs of said first and second circuits.

7. (Original) The signal processing apparatus of claim 6 wherein said second circuit includes a second analog-valued floating-gate transistor operable to effect a time delay on the second signal portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

8. (Previously presented)A signal processing apparatus, comprising:

a signal processing path including two or more signal processing elements; and

a time delay element disposed between adjacent processing elements of the two or more signal processing elements, said time delay element including at least one analog-valued floating-gate field effect transistor,

wherein a time delay of said time delay element depends on an amount of electrical charge stored on the floating gate of the at least one analog-valued floating-gate field effect transistor, said amount of electrical charge adjusting a slew rate of an output of the time delay element to thereby controllably influence a triggering time of at least one of the two or more signal processing elements.

9. (Original) The signal processing apparatus of claim 8, further comprising a combiner configured to receive and combine output signals from said adjacent processing elements.

10. (Previously presented)An apparatus for processing a signal, comprising:

an input node configured to receive a signal;

an intermediate node;

an output node;

a first circuit coupled between said input node and said intermediate node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the signal received at said input node depending on an amount of electrical charge stored on a floating gate of said first transistor; and

a second circuit disposed between said intermediate node and said output node, wherein said amount of electrical charge adjusts a slew rate of an output of the first circuit to thereby controllably influence a triggering time of the second circuit.

11. (Original) The apparatus of claim 10 wherein said second circuit includes a second analog-valued floating-gate transistor operable to effect a time delay on an intermediate signal received at said intermediate node depending on an amount of electrical charge stored on a floating gate of said second transistor.

12. (Previously presented)An apparatus for processing a signal, comprising:

an input node configured to receive an input signal;

a splitter operable to split the input signal into at least a first signal portion and a second signal portion and direct the first signal portion to a first node and direct the second signal portion to a second node;

a first circuit coupled between said first node and a third node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an amount of electrical charge stored on a floating gate of said first transistor, said amount of electrical charge stored on the floating gate of said first transistor adjusting a slew rate of an output of the first circuit to thereby controllably influence a triggering time of a circuit connected to the third node; and

a second circuit coupled between said second node and a fourth node, said second circuit including a second analog-valued floating-gate transistor operable to effect a time delay on the second signal portion received depending on an amount of electrical charge stored on a

floating gate of said second transistor, said amount of electrical charge stored on the floating gate of said second transistor adjusting a slew rate of an output of the second circuit to thereby controllably influence a triggering time of a circuit connected to the fourth node.

13. (Previously presented)A method of processing a signal, comprising:

receiving an input signal at an input node;

splitting said input signal into a first portion and a second portion;

processing said first portion using a first circuit comprising a first analog-valued floating-gate transistor, said step of processing said first portion including effecting a time delay on said first portion depending on an amount of electrical charge stored on a floating gate of said first transistor, said amount of electrical charge adjusting a slew rate of an output of a delay structure associated with the floating-gate transistor to thereby controllably influence a triggering time of a circuit connected to the delay structure; and

processing said second portion.

14. (Original) The method of claim 13, further comprising a step of combining the processed first and second portions.

15. (Original) The method of claim 13 wherein the step of processing said second portion includes using a second circuit comprising a second analog-valued floating-gate transistor, said second step of processing said second portion including effecting a time delay on said second portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

16. (Previously presented)A method of processing a signal, comprising:

processing an input signal into an intermediate signal using a first circuit comprising a first analog-valued floating-gate transistor, said step of processing said input signal including effecting a time delay on said input signal depending an amount of electrical charge stored on a floating gate of said first transistor; and

processing said intermediate signal into an output signal,

wherein said amount of electrical charge adjusts a slew rate of an output of a delay structure associated with the floating-gate transistor to thereby controllably influence a triggering time of a circuit connected to the delay structure.

17. (Original) The method of claim 16 wherein said step of processing said intermediate signal includes using a second circuit comprising a second analog-valued floating-gate transistor, said step of processing said intermediate signal including effecting a time delay on said intermediate signal depending on an amount of electrical charge stored on a floating gate of said second transistor.

18 – 26. (Canceled)

27. (Previously presented)A signal processing apparatus, comprising:

means for receiving an input signal at an input node;

means for splitting said input signal into a first portion and a second portion;

means for processing said first portion using a first circuit comprising a first analog-valued floating-gate transistor, said means for processing said first portion including effecting a time delay on said first portion depending on an amount of electrical charge stored on a floating gate of said first transistor; and

means for processing said second portion,

wherein said amount of electrical charge adjusts a slew rate of an output of a delay means associated with the floating-gate transistor to thereby controllably influence a triggering time of a circuit connected to the delay means.

28. (Original) The signal processing apparatus of claim 27, further comprising means for combining the processed first and second portions.

29. (Original) The signal processing apparatus of claim 27 wherein the means for processing said second portion includes using a second circuit comprising a second analog-valued floating-gate transistor, said means for processing said second portion including affecting a time delay on said second portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

30. (Previously presented)A signal processing apparatus, comprising:

means for processing an input signal into an intermediate signal using a first circuit comprising a first analog-valued floating-gate transistor, said means for processing said input signal including effecting a time delay on said input signal depending on an amount of electrical charge stored on a floating gate of said first transistor; and

means for processing said intermediate signal into an output signal,

wherein said amount of electrical charge adjusts a slew rate of an output of a delay means associated with the floating-gate transistor to thereby controllably influence a triggering time of a circuit connected to the delay means.

31. (Original) The signal processing apparatus of claim 30 wherein said means for processing said intermediate signal includes using a second circuit comprising a second analog-valued floating-gate transistor, said means for processing said intermediate signal including effecting a time delay on said intermediate signal depending on an amount of electrical charge stored on a floating gate of said second transistor.

32. (Previously presented)A signal processing apparatus, comprising:

a time-interleaved system having two or more signal processing pathways, each signal processing pathway configured to receive a common input signal; and

one or more delay structures disposed in one or more of said two or more signal processing pathways, each delay structure including at least one floating-gate field effect transistor having a floating gate adapted store an amount of electrical charge so as to adjust a slew rate of an output of the delay structure to thereby controllably influence a triggering time of a circuit connected to the delay structure.

33 – 36. (Canceled)

37. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit,

~~The signal processing apparatus of claim 33~~ wherein the circuit comprises a pipelined circuit.

38. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit,

~~The signal processing apparatus of claim 33~~ wherein the circuit comprises a time-interleaved circuit.

39. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit,

~~The signal processing apparatus of claim 33~~ wherein the circuit comprises an analog-to-digital converter.

40. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit, wherein the first and second circuit characteristics correspond to relative delays presented to signals transmitted in the first and second circuit pathways

~~The signal processing apparatus of claim 34~~ wherein the circuit comprises an analog-to-digital converter.

41. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit, said first and second circuit characteristics corresponding to relative gains of circuit elements in the first and second circuit pathways.

~~The signal processing apparatus of claim 35~~ wherein the circuit comprises an analog-to-digital converter and wherein the first and second circuit pathways are clock generating pathways to respective first and second track-and-hold circuits of the analog-to-digital converter.

42. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit,

~~The signal processing apparatus of claim 33~~ wherein the circuit comprises a digital-to-analog converter.

43. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit, said first and second circuit characteristics corresponding to relative gains of circuit elements in the first and second circuit pathways,

~~The signal processing apparatus of claim 35~~ wherein the circuit comprises a digital-to-analog converter.

44. (Currently amended) A signal processing apparatus, comprising:

an electrical circuit; and

a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,

wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit,

~~The signal processing apparatus of claim 33~~ wherein the charge stored on the floating gate can be modified during operation of the circuit.

45 – 46. (Canceled)

47. (Previously presented)A signal processing apparatus, comprising:

means for receiving an input signal at an input node of a circuit;

means for splitting the input signal into first and second circuit paths of said circuit;

a floating-gate field effect transistor disposed in the first circuit path; and

means for modifying a first circuit characteristic in the first circuit path relative to a second circuit characteristic in the second circuit path by adjusting an amount of charge stored on a floating of the floating-gate field effect transistor, wherein the first circuit characteristic comprises a gain of a circuit element disposed in the first circuit path.

48. (Previously presented)A signal processing apparatus, comprising:

means for receiving an input signal at an input node of a circuit;

means for splitting the input signal into first and second circuit paths of said circuit;

a floating-gate field effect transistor disposed in the first circuit path; and

means for modifying a first circuit characteristic in the first circuit path relative to a second circuit characteristic in the second circuit path by adjusting an amount of charge stored on a floating of the floating-gate field effect transistor, wherein the first circuit characteristic relates to frequency response, offset or transfer function of the first circuit path.

49. (Currently amended) The signal processing apparatus of claim ~~45~~ 47 wherein the circuit comprises a pipelined circuit.

50. (Currently amended) The signal processing apparatus of claim ~~45~~ 47 wherein the circuit comprises a time-interleaved circuit.

51. (Currently amended) The signal processing apparatus of claim ~~45~~ 47 wherein the means for modifying is operational during times when the signal processing apparatus is operating.